# REMARKS

Claims 1-38 were pending in the application. Claims 1, 9, 17, 25, 33, 37 and 38 have been amended. No claims have been added or canceled. Accordingly, claims 1-38 remain pending subsequent entry of the present amendment.

## Specification

The specification has been amended to update the related application numbers.

## Drawings

Figures 1A, 1B, 2A, and 2B have been revised to include a prior art label.

## 35 U.S.C. § 101 Rejections

In the present Office Action, claims 33-38 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Specifically, the Office Action states the "claims are directed to a signal directly or indirectly by claiming a medium" and there is evidence in the Specification that a computer readable medium is defined as a transmission medium, such as a carrier wave. It is believed in the Office Action that the claims are directed to a form of energy, which does not fall in the category of invention.

Independent claim 33 is directed to a digital storage medium and is therefore believed statutory. Claim 37 has been amended to recite a computer-readable storage medium and is also believed statutory. Finally, claim 38 has been cancelled.

## 35 U.S.C. § 112 Rejections

In the present Office Action, claims 33-38 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 9, 11, 17, 25, and 38 have been amended in a manner believed to overcome the rejections. In particular, claim 1 has been amended to correct an antecedent basis issue. Claims 1, 9, 17, 25 and 37 have been amended to indicate N and M are integers. Additionally, the term "block" has been clarified in claim 11.

## 35 U.S.C. § 103 Rejections

In the present Office Action, claims 1-3, 5, 7, 9-11, 13, 15, 17-19, 21, 23, 25-27, 29, 31, 33, and 36-38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Publication Number 2004/0015684 (hereinafter "Peterson"). Claims 6, 8, 14, 16, 22, 24, 30, 32, and 35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Peterson in view of Applicant's Admitted Prior Art (AAPA). Claims 4, 12, 20, 28, and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Peterson in view of U.S. Patent Number 4,860,190 (hereinafter "Kaneda"). However, Applicant submits each of the pending claims recite features that are neither disclosed nor suggested by the combination of cited references. Accordingly, Applicant traverses the above rejections and requests reconsideration.

Amended claim 1 recites a mechanism for assuring quality of service for a context in a digital processor comprising "a first scheduling register dedicated to the context and having N out of M bits set, said bits being indicative of a pattern for assigning instruction issue slots for the context". In the present Office Action, it is suggested that these features are disclosed by Peterson in paragraph 0034 and FIG. 4C. However, register 337 in FIG. 4A-4C of Peterson is not dedicated to a context. Rather, several thread identifiers may be loaded into thread scheduling register 337 as shown in FIG. 4B-4C and described in paragraphs 0032-0034.

Also, claim 1 recites the register has N out of M bits set. The amended claim further specifies the bits are "indicative of a pattern for assigning instruction issue slots for the context". In Peterson, the bits are set in order to specify thread identifiers for multiple threads. The bits in Peterson are not set for a single context. Further, a bit in Peterson does not indicate a pattern for assigning instruction issue slots for the context. A bit in Peterson is part of a register entry 420, wherein each entry 420 has 4 bits in the examples shown in FIG. 4A-4C to denote a thread identifier. The thread identifier values within the entries 420 specify an execution order, but not each bit as recited in the claim. Also, register 337 has several thread identifier values and is not dedicated to one thread. For at least these reasons, claim 1 is patently distinct from the cited art taken alone or in combination.

In addition to the above, claim 1 recites "a first scheduler that consults the bits sequentially to assign issue slots to the context according to whether a bit is set or not set". In Peterson, register 337 is read by the processor circuitry 320 of FIG. 3 in order to allocate execution within circuitry 320. However, as disclosed in paragraph 0032, the circuitry 320 accesses the entries 420 sequentially and not the bits as recited. Also, the circuitry 320 does not assign issue slots for a context according to whether a bit is set or not set. Circuitry 320 must determine the value of the entire entry 420 and not a single bit in order to determine which thread to execute. For these further reasons claim 1 is patently distinguishable from the cited art. As independent claims 9, 17, 25, 33, 37 and 38 include features similar to claim 1, these claims are patentably distinguished from the cited references for similar reasons. As each of the dependent claims include the features of the independent claims on which they depend, each of the dependent claims are patentably distinct for at least the above reasons.

Still further, the dependent claims recite additional features neither disclosed nor suggested by the cited art. For example, claim 3 recites "the number of N bits determines the proportion of issue slots assigned to the context". In the present Office Action, it is suggested that paragraph 0034 of Peterson discloses these features. However, in contrast to the presently claimed invention, the allocation of execution time for a particular thread in Peterson is determined by the number of entries 420 within register 337 that have the corresponding thread identifier value. Also, in claim 3, the number of N bits all correspond to a dedicated context. This is not true in Peterson, since the bits are used to specify a thread identifier. For these further reasons, claim 3 is patently distinguishable from the cited art.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In the present case, Applicant submits for reasons stated above that the prior art does not teach or suggest all of the limitations of at least the independent claims. Accordingly, Applicant submits a prima facie case of obviousness has not been established. Applicant submits all pending claims are patentably distinct from the cited art and withdrawal of the rejections is respectfully requested.

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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